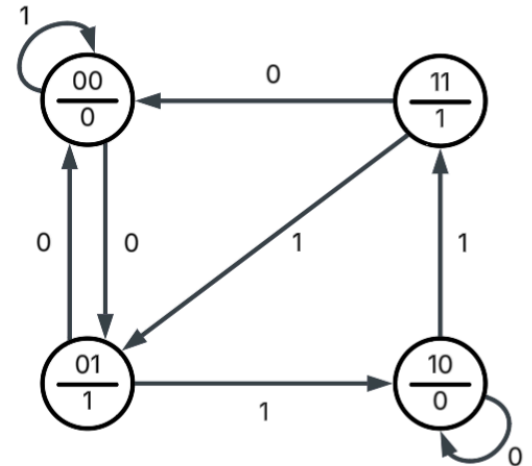


ANSWER KEY

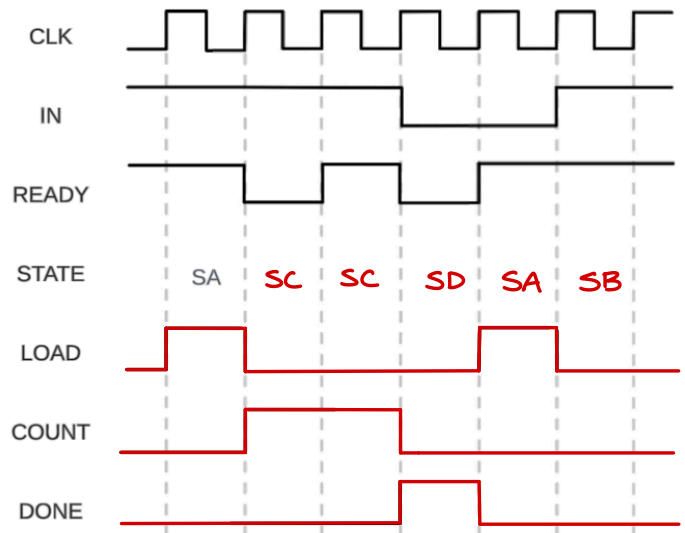
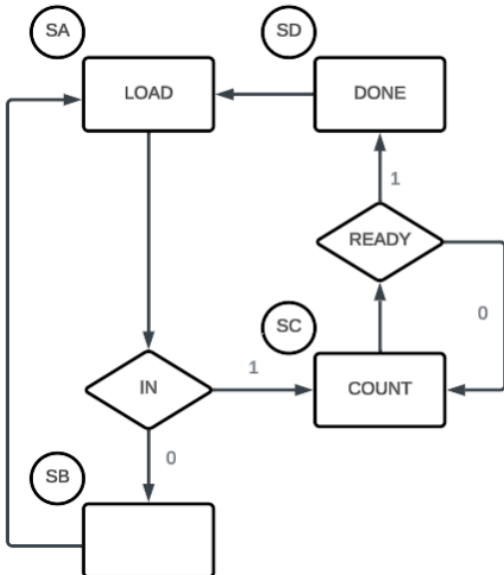
HW5: State Machine Behavior

1. Complete the next state truth table for the following FSM diagram. Begin at S0.

| Q1 | Q0 | IN | D1 | D0 | OUT |
|----|----|----|----|----|-----|
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 |

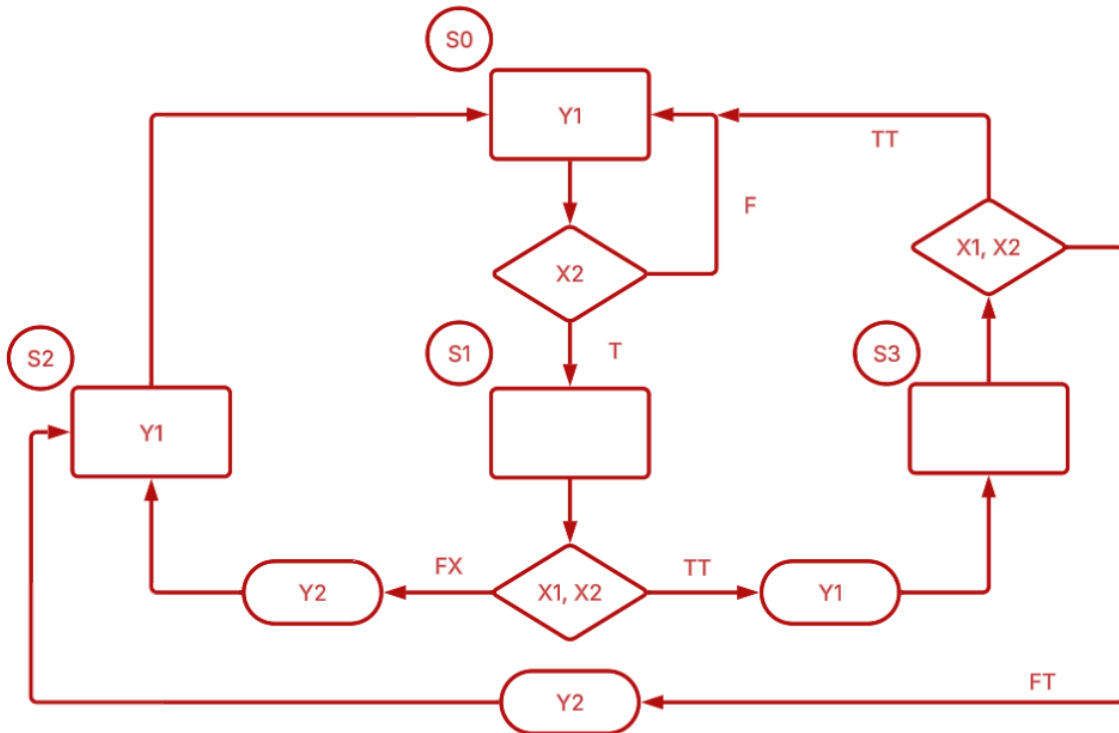
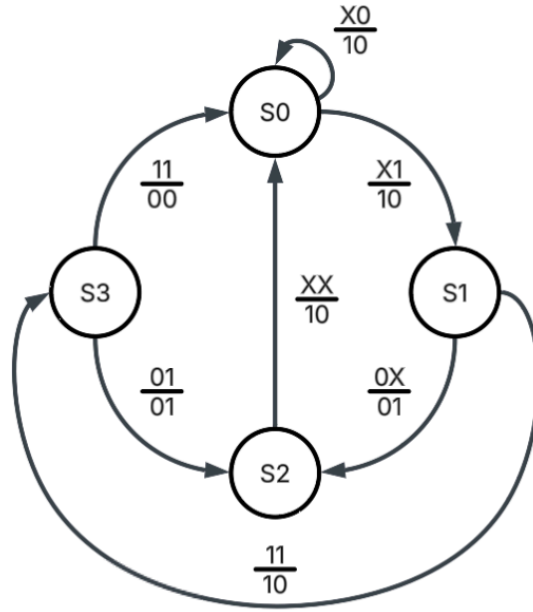


2. Given the ASM chart, complete the corresponding timing diagram.



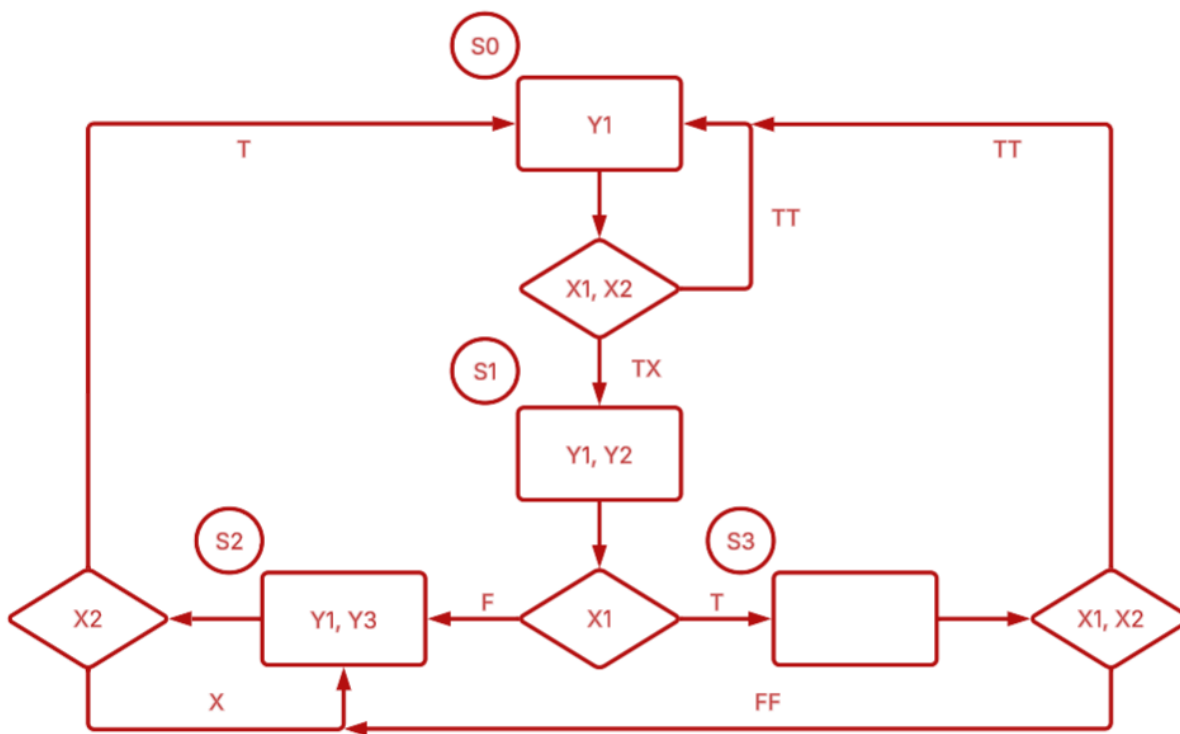
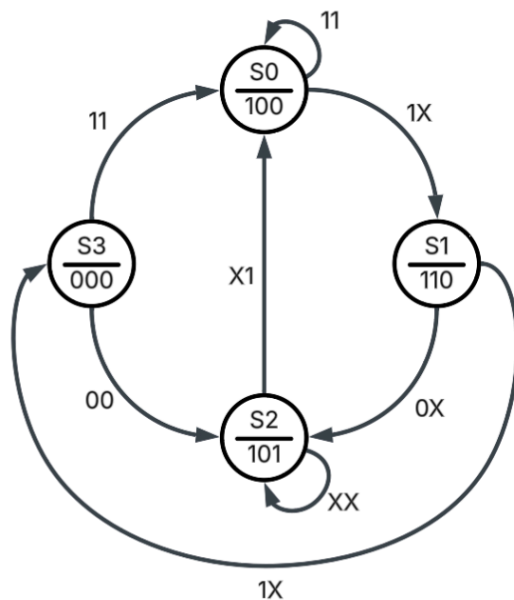
3. Convert the Mealy state graph into an ASM chart given the following:

- Inputs: X1, X2
- Outputs: Y1, Y2



4. Convert the Moore state graph into an ASM chart given the following:

- Inputs: X1, X2
- Outputs: Y1, Y2, Y3



5. A lock is controlled by a Mealy FSM and unlocks when a code is entered in the correct sequence. The system uses the following inputs and outputs:
- Inputs: A, B, C
 - Outputs: U, R (U = 1 means the safe unlocks, R = 1 means the sequence is invalid)

If at any point the sequence is incorrect, the FSM will reset and output to X to indicate an invalid code. The safe unlocks when the buttons A, B, C are pressed in that exact order.

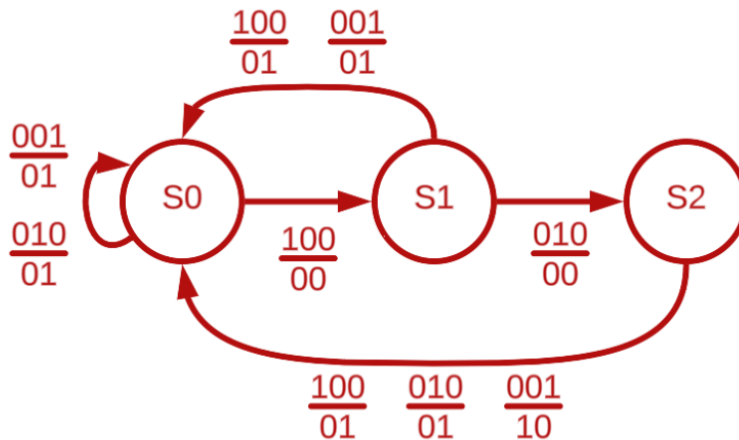
- a. Calculate the total ROM size.

2 bits for current state (00, 01, 10)
 ROM address size = 5
 $2^5 = 32 \leftarrow$ ROM size/entries
 2 bits for current state + 2 bits for U & R
 4 bits/word
 total ROM = $32(4) = 128$ bits

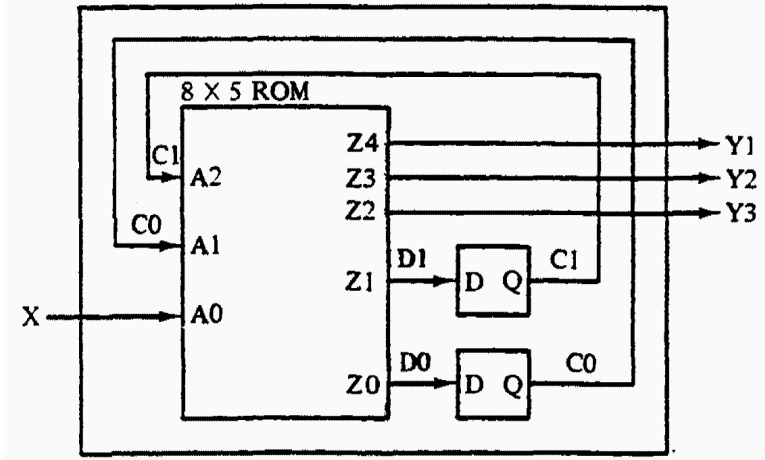
- b. How many flip-flops are required for the register?

3 states \rightarrow 00, 01, 10
 2 flip-flops

- c. Design the corresponding Mealy FSM.



6. Given the block diagram design of a controller based on the ROM method and with D flip-flops, derive the corresponding ASM chart.



| Contents of the ROM | |
|---------------------|----------|
| Location | Contents |
| 0 | 11H |
| 1 | 11H |
| 2 | 16H |
| 3 | 0FH |
| 4 | 00H |
| 5 | 00H |
| 6 | 04H |
| 7 | 04H |

| A2 | A1 | A0 | ROM location | content | Z4 | Z3 | Z2 | Z1 | Z0 |
|----|----|----|--------------|---------|----|----|----|-----|-----|
| C1 | C0 | X | | | Y1 | Y2 | Y3 | C1+ | C0+ |
| 0 | 0 | 0 | 0 | 11H | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 11H | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 2 | 16H | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 3 | 0FH | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 4 | 00H | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 5 | 00H | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 6 | 04H | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 7 | 04H | 0 | 0 | 1 | 0 | 0 |

