UF Herbert Wertheim College of Engineering
Department of Electrical & Computer Engineering
UNIVERSITY of FLORIDA

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EEL3701C - Fall 2025

HW6: VHDL Testbenches

Setup:

1. Make sure to download **all** the necessary files from our website. You should have downloaded 5 files total: hw6_1.vhd, hw6_1_tb.vhd, hw6_2a.vho, hw6_2b.vho and hw6_2_tb_template.vhd.
2. Watch the following video on how to set up and simulate in a ModelSim project: https://youtu.be/hOuJcmq42cU. If you experience any issues, make sure to watch the video again in case there is something you missed. This is particularly true for setting the language to VHDL 2008 and restarting simulations after changing architectures.
3. Import all files into your ModelSim project (being sure to copy them to the project directory), then compile once or twice. It may be useful to use an external editor such as Notepad++ or Visual Studio Code when modifying the VHDL files, but ModelSim will work too. Be sure that if you try to modify a file with ModelSim, you right-click and uncheck Read-Only before you edit the file.
4. At the end, you will need to submit a PDF file with everything required and your updated hw6_2_tb_template.vhd file.

Part 1 Questions:

1. Analyze the behavior of hw6_1.vhd. What type of logic gate is it implementing? What does the incorrect implementation do wrong?
2. Simulate hw6_1_tb.vhd with the “correct” architecture. Take a screenshot of the simulation and show at least one correct case, annotating why it is correct.
3. Simulate hw6_1_tb.vhd with the “incorrect” architecture. Take a screenshot of the simulation and show at least one incorrect case, annotating why it is incorrect. Afterwards, take a screenshot of the output window showing the number of incorrect test cases, as well as at least one output showing the expected and actual value.
4. To submit:
    a. Answers to Question 1
    b. Screenshot of correct simulation + one annotation
    c. Screenshot of incorrect simulation + one annotation
    d. Screenshot of output window showing number of incorrect test cases and expected vs received output.

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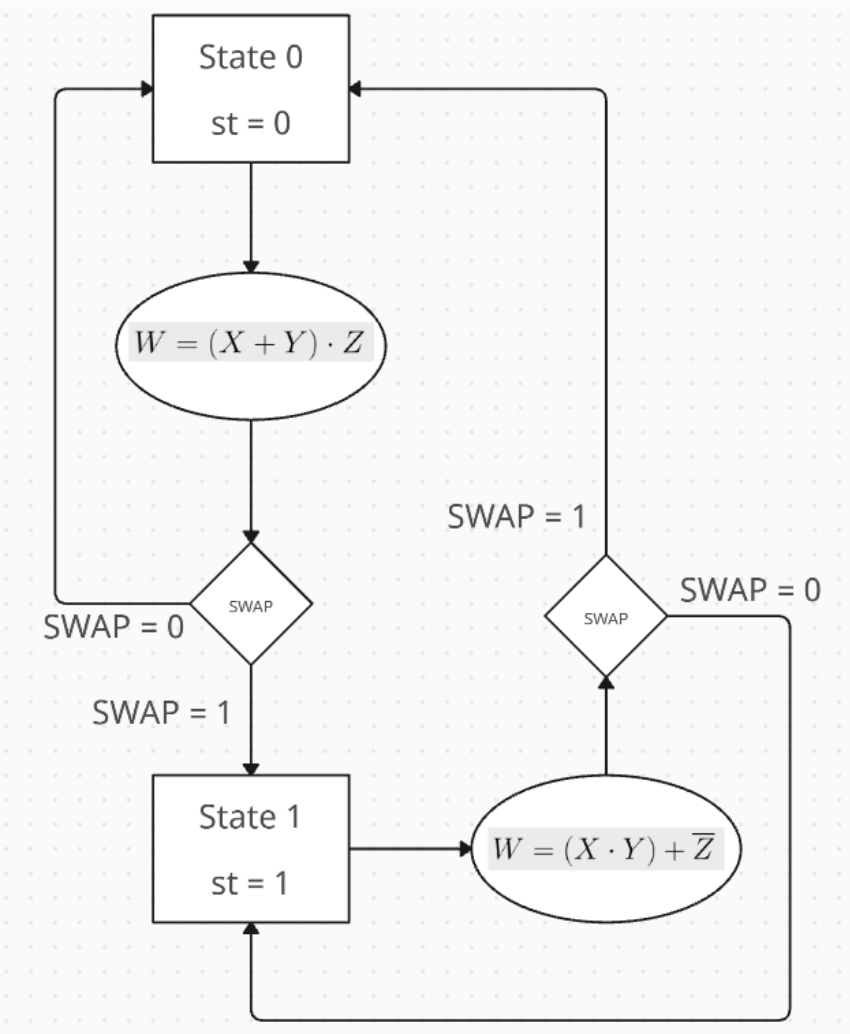
Part 2 Questions:

1. In the previous part, you were told directly which implementation was correct and incorrect. Now, given two implementations of the same FSM, you will determine which one is incorrect and which one is correct.
2. Corresponding FSM behavior (modified ASM, mealy output is an equation):



3. This FSM has two states: State 0 and State 1. When in State 0, W = (X + Y) * Z. When in State 1, W = (X * Y) + !Z. The FSM only switches between the states when SWAP = 1 and there is a rising clock edge. It also has an asynchronous, **active low** reset that brings it back to State 0.

4. Knowing this behavior, it is your goal to figure out which implementation between hw6_2_arch1 and hw6_2_arch2 is correct, and which one is incorrect. Make sure to test the output W of both states. You can assume the **st** output is correct, and accurately tells you what state the FSM is in. Use hw6_2_tb_template.vhd as a guide for how you can begin testing
5. How did you know which one was correct? How did you know which one was incorrect? Submit any screenshots or outputs that support your conclusion. Submit your finalized testbench file as well.
6. To submit:
    a. hw6_2_template.vhd with your changes
    b. Your answer for how you knew which one was correct/incorrect and any supporting screenshots/outputs.