EEL3701C, Exam 1 (Fall 2025)

Digital Logic & Computer Systems
October 14, 2025

Name: _____

UFID: _____

Honor Code:
To receive credit for this exam, you must agree to the following pledge:
On my honor, I have neither given nor received unauthorized aid in doing this assignment. NOTE: UF's Honor Code includes copyright infringement. Providing information to anyone else - even a third party - is a violation of the Honor Code and copyright law.

If you agree to the honor code, please sign below:

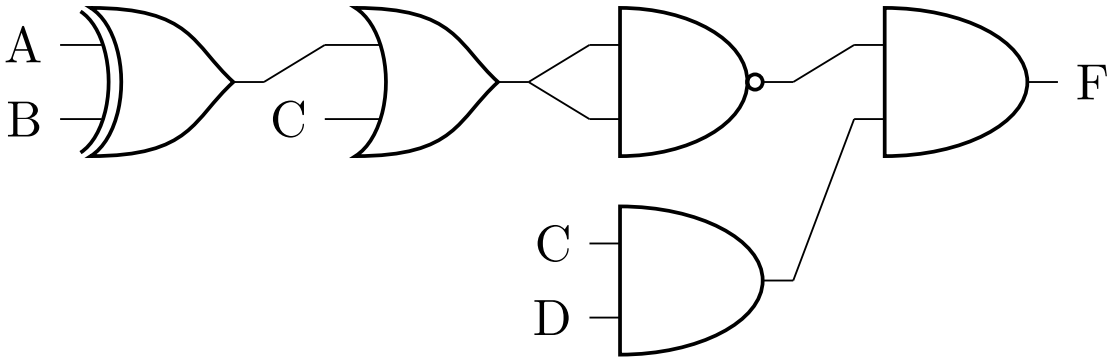
_____

Read all of the following information before starting the exam:

- Show all work, clearly and in order, if you want to get full credit. We reserve the right to take off points if we cannot see how you arrived at your answer (even if your final answer is correct).
- Circle or otherwise indicate your final answers.
- This test has 13 problems that total to 100 points.
- You have 110 minutes (8:20 PM- 10:10 PM) to complete.

Question 1: (7 pts)

Derive the equation for this circuit without simplifying the equation except for the use of the idempotent law (A AND A = A, A OR A = A).



Question 2: (6 pts)

Simplify the following Boolean algebra expression: $\overline{A + (B \cdot C)} \cdot \overline{(\overline{A} \cdot B) + B}$

Question 3: (5 pts)

Given the following VHDL statement, create a circuit diagram. Do **NOT** simplify the equation. Make sure that your input and output names match the statement.

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F <= A and (B or not C) and (not (C or B));
```

Question 4: (5 pts)

Convert 79_{10} to base 3 using any method.

Question 5: (5 pts)

Convert $0xA5F4B1$ into binary.

Question 6: (7 pts)

For the K-Map in Figure 1, answer the following:

6a. Find the MSOP expression (show groupings) (2 pts)

6b. Find MPOS expression (show groupings) (2 pts)

6c. Are your solutions unique, or are there other minimum expressions? Why? (2 pts)

6d. Does the MPOS = MSOP? (1 pt)

CD / AB	00	01	11	10
00	1	0	0	X
01	0	1	1	0
11	0	X	X	1
10	1	0	X	X

Figure 1: 4 Variable K-Map

Question 7: (5 pts)

A decoder with 3 inputs will typically have how many outputs?

A. 3

B. 2

C. 8

D. 4

Question 8: (5 pts)

If a multiplexer has 17 inputs, how many select lines would it need?

A. 4

B. 5

C. 17

D. 6

Question 9: (5 pts)

For a counter that wants to count 7 different values, what is the **minimum** number of flip-flops required?

A. 2

B. 3

C. 1

D. 4

Question 10: (5 pts)

A digital circuit consists of three logic gates connected in series: an AND gate, an OR gate, and a NOT gate. The propagation delays of the gates are as follows:

AND 5 ns

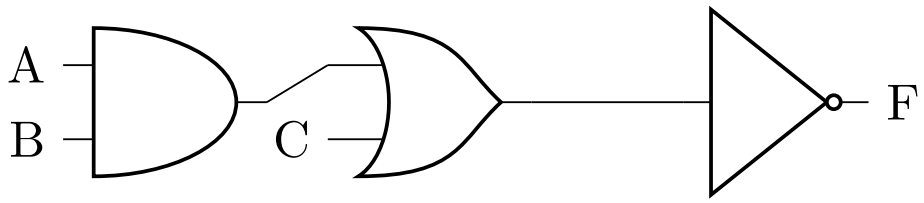
OR 8 ns

NOT 2 ns

10a. What is propagation delay? (1 pt)

10b. Calculate the **total propagation delay** from the input of the AND gate to the output of the NOT gate. (2 pts)

10c. If inputs are fed into the circuit every 10 ns, will the output always settle before the next input change? (2 pts)



Question 11: (15 pts)

Given 4x1 multiplexers and 2x1 multiplexers, create the circuit design for a 10x1 multiplexer. The inputs to the 10x1 are X0 - X9 and the select lines are S0 - S3, with S3 being the most significant bit. For select inputs greater than 1001, the output does not matter.

Question 12: (10 pts)

Answer each of the following questions and make it clear which part is being answered:

12a. When can the output of a latch with an enable change? (4)

12b. When can the output of a flip-flop change? (3)

12c. Why is a JK-FF generally preferred over an SR-FF? (3)

Question 13: (20 pts)

Create a two-bit counter that counts in the order $0 \rightarrow 2 \rightarrow 3 \rightarrow 1$ using T-FFs for all state bits. Use the **minimum** number of flip-flops for this counter. There should be an asynchronous reset that sets the counter to 0. You need to fill in the NSTT, derive the flip-flop inputs using K-maps, then draw a circuit diagram including the flip-flops. Leave any rows or columns deemed unnecessary in the NSTT blank. Fill in the NSTT on this page. Then, derive your equations using K-maps and draw the circuit diagrams on the next page.

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0

Question 13 (continued): (20 pts)

Fill in the NSTT on the previous page. Then, derive your equations using K-maps and draw the circuit diagrams on this page.

EXAM OVER!! GOOD JOB!!

For Instructor Grading purposes only:

QUESTION NO.	POINTS EARNED	MAX POINTS
1		7
2		6
3		5
4		5
5		5
6		7
7		5
8		5
9		5
10		5
11		15
12		10
13		20
Total		100

Scratch Paper